[SINGLE-POLY EEPROM]

Abstract of Disclosure

A single-poly EEPROM is disclosed. The single-poly EEPROM includes a first PMOS transistor that is serially connected to a second PMOS transistor. The first and second PMOS transistors are both formed on an N-well of a P-type substrate. The first PMOS transistor includes a floating gate, a first P^{+} doped drain region, and a first P^{+} doped source region. The second PMOS transistor includes a gate and second P^{+} doped source region. The first P^{+} doped drain region of the first PMOS transistor serves as a drain of the second PMOS transistor. An erase gate extending to the floating gate for erasing the single-poly EEPROM is provided in the P-type substrate.

Figures